CLAIMS:

1. comparator with hysteresis comprising a first transistor (M1) whose gate forms the one input of the comparator and a second transistor (M2) whose gate forms the other input of the comparator, the main current paths of both transistors (M1, M2) being connected to each other at one end, characterized by a third transistor (M3) and a fourth transistor (M4) being provided, the gate of said third transistor (M3) being connected to the gate of said first transistor (M1) and its main current path being circuited between the one end of the main current paths of said first and second transistor (M1, M2) and connected via the main current path of said fourth transistor (M4) to the other end of said main current path of said second transistor (M2), and the gate of said fourth transistor being connected to the output signal or inverted output signal of said comparator.

2. The comparator as set forth in claim 1 wherein said transistors (M1, M2, M3, M4) are bipolar transistors.

3. The comparator as set forth in claim 1 wherein said transistors (M1, M2, M3, M4) are MOS-FETs.

4. The comparator as set forth in claim 3 wherein the width/length ratio of said first transistor (M1) is larger than the width/length ratio of said third transistor (M3).

5. The comparator as set forth in claim 1 comprising, in addition, a fifth transistor (M11) and a sixth transistor (M12), the gate of said fifth transistor (M11) being connected to the gate of said second transistor (M2) and its main current path being circuited between the one end of the main current path of said first and said second transistor (M1, M2) and via the main current path of said sixth transistor (M12), the other end of the main current path of said first transistor (M1) and the gate of said sixth transistor (M12) being connected to the output signal of said comparator when the gate of said fourth transistor (M4) is connected to the inverted output signal of said comparator and the gate of said sixth transistor (M12) being connected to the inverted

output signal of said comparator, when the gate of said fourth transistor (M4) is connected to the output signal of said comparator.

6. The comparator as set forth in claim 4 comprising, in addition, a fifth transistor (M11) and a sixth transistor (M12), the gate of said fifth transistor (M11) being connected to the gate of said second transistor (M2) and its main current path being circuited between the one end of the main current path of said first and said second transistor (M1, M2) and via the main current path of said sixth transistor (M12), the other end of the main current path of said first transistor (M1) and the gate of said sixth transistor (M12) being connected to the output signal of said comparator when the gate of said fourth transistor (M4) is connected to the inverted output signal of said comparator and the gate of said sixth transistor (M12) being connected to the inverted output signal of said comparator, when the gate of said fourth transistor (M4) is connected to the output signal of said comparator.

7. The comparator as set forth in claim 5 wherein, in addition, a sub-circuit is provided which ensures that said status of the output signal of said comparator is locked even when the voltage level at the one and/or other input of said comparator disappears.

8. The comparator as set forth in claim 5 wherein the one end of said main current path of said first transistor and of said second transistor is connected to a current source.

9. The comparator as set forth in claim 5 wherein the one end of said main current path of said first transistor and the main current path of said second transistor is connected in each case via the main current path of the other transistor to a supply voltage.

10. An ASK demodulator comprising a comparator with hysteresis comprising:

a first transistor (M1) whose gate forms the one input of the comparator and a second transistor (M2) whose gate forms the other input of the comparator, the main current paths of both transistors (M1, M2) being connected to each other at one end, characterized by a third transistor (M3) and a fourth transistor (M4) being provided, the gate of said third transistor (M3) being connected to the gate of said first transistor (M1) and its main current path being circuited between the one end of the main current paths of said first and second transistor (M1, M2) and connected via the main current path of said fourth transistor (M4) to the other end of said main current path of said second transistor (M2), and the gate of said fourth transistor being connected to the output signal or inverted output signal of said comparator.

11. The ASK demodulator as set forth in claim 10 further comprising, a rectifier (2, C1) whose output (5) is connected to a first voltage follower (6) whose output is connected to a first capacitor (C2) and connected to a second voltage follower (7) whose output is connected to a second capacitor (C2), the capacitance of which is smaller than the capacitance of said first capacitor (C2), said first capacitor (C2) being connected to the one input and said second capacitor (C3) being connected to the other input of said comparator (8).

12. The ASK demodulator as set forth in claim 11 wherein said two voltage followers (6, 7) each comprise opposing offset voltages.

13. The ASK demodulator as set forth in claim 12 wherein said comparator (8) comprises an offset voltage.